

REMARKS

Applicant thanks the Examiner for indicating that claims 7-16 are allowed. Claims 1-53 are pending, with claims 17-46 being withdrawn and claims 1, 2, 3, 4, 7, 17, 27, 37, 47, 49, and 51 being independent. Claims 51-53 are newly presented. Support for these new claims can be found in the originally-filed specification at least at Fig. 1 and the accompanying text. No new matter has been added.

Claims 1-6 and 47-50 have been rejected under 35 U.S.C. §112, second paragraph. Applicant has amended claims 1-4 to specify that the transistor supplies a first current "in a driving period" and a second current is flowed to the transistor in a "precharging period." Accordingly, applicant requests withdrawal of the rejection of claims 1-4, and of claims 5 and 6, which depend from claim 4.

Applicant has amended claims 47 and 49 in accordance with the Examiner's suggestions. Accordingly, applicant requests withdrawal of the rejection of claims 47 and 49, and claims 48 and 50, which depend from claims 47 and 49, respectively.

Claims 1, 4, and 47-50 have been rejected as being anticipated by U.S. Patent No. 6,710,995 (Knoedgen). Applicant requests withdrawal of this rejection for the following reasons.

Knoedgen relates to a circuit for protecting a battery from overcurrent conditions. See Knoedgen at col. 1, lines 7-10 and col. 2, lines 32-34 and Fig. 2. Knoedgen's circuit includes a collection of cells 81, 82, and 83 coupled in parallel between the negative terminal of the battery 70 through a fuse 104, 108, or 112, and the ground of the load 143. See Knoedgen at col. 2, lines 38-44 and Fig. 2. The cell 81 includes a zener effect device 116 and a switch 120 connected in parallel with the zener effect device 116. See Knoedgen at col. 2, line 59 to col. 3, line 7 and Fig. 2. As Knoedgen explains, during normal operation, the switch 120 is ON and during an error condition, the switch is turned OFF. See Knoedgen at col. 3, lines 25-45 and Fig. 2. The switch 120 can be a transistor M1 198. See Knoedgen at col. 3, line 61 to col. 4, line 8 and Fig. 3.

Independent claim 1 recites a semiconductor device including a transistor that supplies a first current to a load in a driving period, and a circuit. The circuit makes a potential of a gate terminal of the transistor at a first potential by flowing a second current to the transistor in a precharging period, and makes the potential of the gate terminal of the transistor at a second potential by flowing the first current to the transistor in a programming period.

Independent claim 4 recites a semiconductor device including a transistor and a circuit. The transistor supplies a first current to a load in a driving period. The circuit makes a potential of a gate terminal of the transistor at a first potential by flowing a second current to the transistor in a first precharging period. Additionally, the circuit makes the potential of the gate terminal of the transistor at a second potential by flowing a third current to the transistor in a second precharging period, and makes the potential of the gate terminal of the transistor at a third potential by flowing the first current to the transistor in a programming period.

Applicant requests withdrawal of the rejection of claims 1 and 4 because Knoedgen fails to describe or suggest flowing a first current to the transistor in a programming period, where the first current is also supplied to a load from the transistor in a driving period, and flowing a second current to the transistor in a precharging period. In Knoedgen, the transistor M1 supplies a "fuse" current to the fuse F1 while it is ON, but that fuse current is not applied to the transistor M1 during a period other than the ON period. Moreover, another current is not applied to the transistor M1 during a period other than the period during which the transistor M1 is ON. Rather, during the OFF period, no current is applied to the transistor M1. See Knoedgen at Fig. 2. For at least these reasons, claims 1 and 4 are allowable over Knoedgen.

Independent claim 47 recites a driving method of a semiconductor device. The method includes generating at a gate terminal of a transistor a first voltage required for the transistor to flow a first current, by supplying the first current to the transistor. The method includes generating at the gate terminal of the transistor a second voltage required for the transistor to flow a second current, by supplying the second current to the transistor after generating the first voltage. The method also includes supplying the second current to a load after generating the second voltage.

Independent claim 49 recites a driving method of a semiconductor device. The method includes generating at a gate terminal of a transistor a first voltage required for the transistor to flow a first current, by supplying the first current to the transistor. The method includes generating at the gate terminal of the transistor a second voltage required for the transistor to flow a second current, by supplying the second current to the transistor after generating the first voltage. The method also includes generating at the gate terminal of the transistor a third voltage required for the transistor to flow a third current, by supplying the third current to the transistor after generating the second voltage, and supplying the third current to a load after generating the third voltage.

Applicant requests withdrawal of the rejection of claims 47 and 49 because Knoedgen fails to describe or suggest generating at a gate terminal of a transistor, a second voltage required for the transistor to flow a second current, and doing so by supplying a second current to the transistor after generating a first voltage at the gate terminal of the transistor to flow a first current through the transistor. In Knoedgen, while a voltage is applied to the transistor M1 during the OFF period, no current flows through the transistor M1 during the OFF period. Rather, current only flows through the transistor M1 when the voltage applied to the transistor M1 reaches 5 Volts and the transistor M1 is turned ON. See Knoedgen at col. 4, lines 16-20. At this time, the fuse 190 is blown. See Knoedgen at col. 4, lines 22-29. For at least these reasons, claims 47 and 49 are allowable over Knoedgen. Claims 48 and 50 depend, respectively, from claims 47 and 49, and are allowable for at least the reasons that claims 47 and 49 are allowable.

Claims 2, 3, 5, and 6 have been rejected as being obvious over Knoedgen.

Independent claim 2 recites a semiconductor device including a transistor and a circuit. The transistor supplies a first current to a display element in a driving period. The circuit is for making a potential of a gate terminal of the transistor at a first potential by flowing a second current to the transistor in a precharging period, and is for making the potential of the gate terminal of the transistor at a second potential by flowing the first current to the transistor in a programming period.

Independent claim 3 recites a semiconductor device including a transistor and a circuit. The transistor supplies a first current to a signal line in a driving period. The circuit is for making a potential of a gate terminal of the transistor at a first potential by flowing a second current to the transistor in a precharging period, and is for making the potential of the gate terminal of the transistor at a second potential by flowing the first current to the transistor in a programming period.

Applicant requests withdrawal of the rejection of claims 2 and 3 because, as discussed above with respect to claims 1 and 4, Knoedgen fails to describe or suggest flowing a first current to the transistor in a programming period, where the first current is also supplied to a load from the transistor in a driving period, and flowing a second current to the transistor in a precharging period. For at least these reasons, claims 2 and 3 are allowable over Knoedgen.

Claims 5 and 6 depend from claim 4 and are allowable for at least the reasons that claim 4 is allowable.

New independent claim 51 recites a semiconductor device including a load, a transistor electrically connected to the load, a first current source, and a second current source. A circuit operationally connects any one of a source region and a drain region of the transistor and any one of the first current source and the second current source. The circuit makes a potential of a gate electrode of the transistor at a predetermined potential by electrically connecting the second current source and the any one of the source region and the drain region of the transistor.

Claim 51 is allowable over Knoedgen because Knoedgen fails to describe or suggest a circuit that makes a potential of a gate electrode of a transistor at a predetermined potential by electrically connecting a second current source and any one of a source region and a drain region of the transistor. In Knoedgen, the second current source 206 is connected only to the gate electrode of M1. See Knoedgen at Fig. 3.

Claims 52 and 53 depend from claim 51 and are allowable for at least the reasons that claim 51 is allowable.

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Serial No. : 10/787,347
Filed : February 27, 2004
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Attorney's Docket No.: 12732-212001 / US7008

Enclosed is a \$300.00 check for excess claim fees and a \$120.00 check for a one month Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: November 22, 2005

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